REMARKS

Claims 1-41 are currently pending in connection with the present application. Claims 1, 8, 18, 26, 30 and 39 are independent claims. No claims have been amended, cancelled, or added. There is no new matter. Applicants traverse the rejection set forth in the Office Action dated January 18, 2006.

Drawings

Applicant notes that the Examiner has yet to object or accept the drawings filed on January 13, 2004. Absent such an indication, Applicant assumes that the drawings are accepted. However, an indication of such is earnestly solicited.

Allowable Subject Matter

Applicant appreciates that claims 8-38 and 40 are allowed and that claims 3-7 are objected to as being dependent upon a rejected base claim that would be allowable if rewritten in independent form, including all of the features of the base claim and intervening claims. Applicant notes that these claims are allowable in their own right, and not simply for the reasons set forth in the Office Action. Furthermore, it is submitted that claims 1, 2, 39 and 41 are also allowable in view of the following remarks.

Prior Art Rejections

35 U.S.C. §102(e) Yanagisawa Rejection

Claims 1, 2, 39 and 41 stand rejected under 35 U.S.C. §102(e) as being anticipated by Yanagisawa et al. (U.S. Patent No. 6,525,972). Applicants respectfully traverse this rejection.

Claim 1 recites the feature of "a word line enable circuit for generating a word line enable signal in response to the oscillation signal; and a control circuit for controlling the oscillator circuit and the word line enable circuit so that a pulse width of the word line enable signal is widened as operation mode of the memory device changes from an active mode to a standby mode".

Yanagisawa is directed to a semiconductor memory device having a boosted potential generation circuit. The semiconductor memory device 50 includes a command decoder 1, a row control circuit 4, and a word selection circuit 3, which receives a command from an external device, such as a central processing unit (CPU). When the command decoder 1 receives an instruction, the command decoder 1 activates a control signal indicating that an active command or a refresh command was received. In response, a row control circuit 4 generates a row enable signal RE, activating the word selection circuit 4. Input signals to selection circuit 3 include the row enable signal RE from row control circuit 4, VPP originating from the booster circuit, and an address buffer signal ADD from address buffer 2. FIG. 5 illustrates a timing diagram showing the control signal ACT/REF, row enable signal RE, and boosting control signal PREVBT. When command decoder 1 receives a command that indicates the word line is to be activated, the control signal ACT/REF pulses high,[1] while the row enable signal RE does not pulse. Instead, the row enable signal RE simply stays high to ensure that the memory does not receive multiple instructions while executing a current command.

[1] FIG. 5, time T1.

Thus, the word line may not be activated until the row enable signal returns to low and the memory array 10 has been precharged.[2]

First, Applicant submits that Yanagisawa does not teach, suggest or render obvious "a word line enable circuit **for generating** a word line enable signal **in response** to the oscillation signal," as recited in independent claim 1. On the contrary, Yanagisawa does not teach or suggest that the word selection circuit produces a word line enable signal. While Yanagisawa discloses a row control circuit that controls **both an oscillator and generates a row enable signal**, Yanagisawa does not teach or suggest that the row control circuit produces **an enable signal in response to an oscillation signal**.[3]

Second, Applicant submits that Yanagisawa does not teach, suggest or render obvious "a control circuit for controlling the oscillator circuit and the word line enable circuit so that **a pulse width of the word line enable signal is widened** as operation mode of the memory device changes from an active mode to a standby mode" as recited in independent claim 1. On the contrary, both the command decoder signal and the boosting control signal PREVBT have a fixed pulse width, while the row enable signal RE does not pulse at all.[4] None of the other signals affecting the word selection circuit 3 has a widened pulse width as operation mode of the memory device changes.

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[2] Col. 15, lines 51-55.
[3] On page 3 of the Office Action dated January 18, 2006, the Examiner sets forth that the "row control circuit 4" in Yanagisawa corresponds to Applicant's "control circuit."
[4] FIGS. 5 and 6.

Accordingly, Applicant respectfully submits that Yanagisawa fails to disclose teach, suggest or render obvious each and every feature of independent claim 1 and claim 1 is therefore patentable. For similar reasons, independent claim 39 is also patentable (although claims 1 and 39 should be interpreted solely based upon the limitations set forth therein). Therefore, Applicant requests that the rejection of independent claims 1 and 39 and dependent claims 2 and 41, under 35 U.S.C. §102(e), be withdrawn.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-41 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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